CLAIMS

1. A semiconductor device comprising:
a first electrode component;
a second electrode component;
a first layer comprising at least a portion of the first electrode component and at least a portion of the second electrode component;
a second layer having a portion comprising deposited semiconductor material contacting the first and second electrode components; and
a third layer comprising a substrate,
wherein the first, second and third layers are arranged in order such that the second layer is positioned between the first layer and the third layer and wherein the first and second electrode components comprise electro-deposited metal.

2. A semiconductor device as claimed in claim 1, wherein the first, second and third layers are of respective substantially uniform thicknesses.

3. A semiconductor device as claimed in claim 1 or 2, wherein the third layer fixes the substrate to the semiconductor device.

4. A semiconductor device as claimed in any one of claims 1 to 3, wherein the first layer has a substantially planar surface forming a surface of the semiconductor device incorporating portions of the first and second electrode components.

5. A semiconductor device as claimed in any one of claims 1 to 4, wherein the deposited semiconductor material comprises organic semiconductor material.

6. A semiconductor device as claimed in any one of claims 1 to 5, wherein the deposited semiconductor material comprises indications that it was deposited from liquid.

7. A semiconductor device as claimed in any one of claims 1 to 6, wherein the semiconductor material is embedded in the device and overlain by the first layer.

8. A semiconductor device as claimed in any preceding claim wherein the substrate is flexible.

9. A semiconductor device as claimed in any preceding claim, wherein the device is a thin film transistor having a channel in the semiconductor material, a source electrode as the first electrode, a drain electrode as the second electrode, and a gate electrode, wherein the source, drain and gate electrodes are formed from electro-deposited metal

10. A semiconductor device as claimed in claim 9, wherein the first layer comprises the source electrode and the drain electrode and the gate electrode lies in a fourth layer between the second layer and the third layer.

11. A semiconductor device as claimed in claim 10, wherein the gate electrode of the fourth layer and the semiconductor material of the second layer are aligned.

12. A semiconductor device as claimed in claim 10 or 11, further comprising a fifth layer, comprising a continuous dielectric layer, between the fourth layer and the third layer.

13. A semiconductor device as claimed in claim 12, wherein the fourth and fifth layers are of respective substantially uniform thicknesses.

14. A semiconductor device as claimed in any one of claims 10 to 13, wherein the source and drain electrodes each partially overlap the gate electrode but are separated therefrom by the semiconductor material and dielectric material.

15. A semiconductor device as claimed in any one of claims 10 to 14, wherein the first layer has a substantially planar surface forming a surface of the semiconductor device incorporating portions of the source and drain electrodes, but not the gate electrode.

16. A semiconductor device as claimed in any one of claims 10 to 15, wherein the second layer comprises insulating material forming a well containing the semiconductor material.

17. A semiconductor device as claimed in claim 16, wherein the insulating material is photo-patternable, and the portions of the device underlying the insulating material are photo-transparent.

18. A semiconductor device as claimed in claim 9, wherein the first layer comprises a first portion of the source electrode, a first portion of the drain electrode and the gate electrode.

19 . A semiconductor device as claimed in claim 18, wherein the second layer comprises a second portion of the source electrode contacting the semiconductor material and a second portion of the drain electrode contacting the semiconductor material.

20. A semiconductor device as claimed in claim 19, wherein the source electrode is formed from the first and second portions in the respective first and second layers and the drain electrode is formed from the first and second portions in the respective first and second layers,

21. A semiconductor device as claimed in claim 19 or 20, wherein the first and second portions of the source electrode are aligned and formed from electro-deposited metal, and the first and second portions of the drain electrode are aligned and formed from electro-deposited metal.

22. A semiconductor device as claimed in any one of claims 18 to 21, further comprising dielectric material in the second layer between the semiconductor material and the gate electrode in the first layer.

23. A semiconductor device as claimed in any one of claims 18 to 22, wherein the first layer has a substantially planar surface forming a surface of the semiconductor device incorporating portions of the source, drain and gate electrodes.

24. A substrate for a display device comprising a plurality of semiconductor devices as claimed in any preceding claim.

25. A method for use in forming a layered semiconductor device comprising:
forming a transfer layer on a conductive carrier by at least the deposition of insulating material on the conductive carrier and then the electro-deposition of metal onto at least first and second portions of the conductive carrier, selectively exposed through the insulating material, to form first and second metal portions;
fixing the transfer layer to a substrate portion of the device; and
removing the conductive carrier from the device.

26. A method as claimed in claim 25, wherein the transfer layer comprises a terminal layer of the device.

27. A method as claimed in claims 25 or 26, further comprising passivating the conductive carrier before forming the transfer layer.

28. A method as claimed in any one of claims 25 to 27, wherein the conductive carrier is of substantially uniform thickness.

29. A method as claimed in any one of claims 25 to 28, wherein the step of fixing the transfer layer to a substrate portion embeds semiconductor material within the device.

30. A method as claimed in claim 29, wherein the semiconductor material is part of the substrate portion.

31. A method as claimed in any one of claims 25 to 30, wherein the formation of the substrate portion comprises:
forming a gate transfer layer on a second conductive carrier by depositing insulating material on the second conductive carrier and then electro-depositing metal onto a portion of the second conductive carrier, selectively exposed through the insulating material;
fixing the gate transfer layer to a substrate; and
removing the conductive carrier from the device.

32. A method as claimed in claim 31, further comprising passivating the second conductive carrier before the formation of the gate transfer layer.

33. A method as claimed in claim 32, wherein the second conductive carrier is of substantially uniform thickness..

34. A method as claimed in any one of claims 31 to 33, further comprising fixing the gate transfer layer to the substrate using an adhesive layer.

35. A method as claimed in any one of claims 31 to 34, further comprising forming a dielectric layer over the gate transfer layer after it is fixed to the substrate.

36. A method as claimed in claim 35, further comprising depositing an adhesive insulating layer over the dielectric layer and selectively removing the adhesive insulating layer from over the gate electrode to form a well.

37. A method as claimed in claim 36, wherein the adhesive insulating material is photo-patternable and exposable through the substrate.

38. A method as claimed in claim 36 or 37, further comprising depositing semiconductor material into the well to form the substrate portion of the device for adherence to the transfer layer.

39. A method as claimed in claim 38, wherein the semiconductor material is deposited as a liquid.

40. A method as claimed in claim 39, wherein the semiconductor material is part of the transfer layer.

41. A method as claimed in claim 40, wherein the substrate portion is a flexible substrate.

42. A method as claimed in any one of claims 25 to 29, 40 or 41, wherein the transfer layer is formed by:

a) selectively forming insulating material on portions of the conductive carrier, to expose first, second and third portions of the conductive carrier;

b) electro-depositing metal onto the first, second and third portions of the conductive carrier to form first, second and third metal portions;

c) depositing dielectric material over at least the second metal portion;

d) electro depositing metal on the first and third metal portions; and

e) depositing semiconductor material over the dielectric layer.

43. A method as claimed in claim 42, wherein the semiconductor material deposited in step e) is selectively deposited between the metal deposited in step d).

44. A method as claimed in claim 42, wherein the step e) precedes step d).

45. A method as claimed in any one of claims 42 to 44, wherein the semiconductor material is initially deposited in liquid form.

46. A method as claimed in any one of claims 42 to 45, wherein the step of fixing the transfer layer to the substrate portion involves the application of a curable adhesive layer to the substrate portion, the contacting of the curable adhesive layer and the transfer layer and the curing of the adhesive.

47. A semiconductor device made in accordance with the method as claimed in any one of claims 25 to 46, wherein the first metal portion and the second metal portion respectively form at least a portion of a first electrode component of the semiconductor device and at least a portion of a second electrode component of the semiconductor device.

48. A transistor device made in accordance with the method as claimed in claim 31, wherein the first metal portion and the second metal portion respectively form at least a portion of a first electrode component of the transistor device and at least a portion of a second electrode component of the transistor device and the metal portion of the gate transfer layer forms a gate electrode of the transistor device.

49. A method for use in forming a transistor device including a source electrode, a drain electrode and a gate electrode comprising:
electro-depositing metal to form at least a portion of the gate electrode;
electro-depositing metal to form simultaneously at least portions of the source electrode and the drain electrode;
depositing semiconductor material;
transferring at least the source electrode and drain electrode to a substrate.

50. A method as claimed in claim 49, wherein the step of transferring encloses the semiconductor material.

51. A method as claimed in claim 49 or 50, wherein the step of transferring creates a substantially planar surface for the transistor device including at least portions of the source electrode and drain electrode.

52. A method as claimed in claim 49, 50 or 51, wherein the source electrode and drain electrode are formed in a first portion of the transistor device that is transferred to a second portion of the transistor device to complete the transistor device, wherein the second portion includes a substrate, the gate electrode and the semiconductor material.

53. A method as claimed in claim 52, wherein the semiconductor material is within a well formed by insulating material that adheres the first and second portions of the transistor device.

54. A method as claimed in claim 49, 50 or 51, wherein the source electrode, drain electrode and gate electrode are formed in a first portion of the transistor device that is transferred to a substrate to complete the transistor device.

55. A method as claimed in claim 54, wherein the step of transferring creates a substantially planar surface for the transistor device including at least portions of the source electrode, the drain electrode and the gate electrode.

56. A transistor device made in accordance with the method as claimed in any one of claims 49 to 56.

57. A device or method substantially as hereinbefore described with reference to and/or as shown in the accompanying drawings.

58. Any novel subject matter or combination including novel subject matter disclosed, whether or not within the scope of or relating to the same invention as the preceding claims.